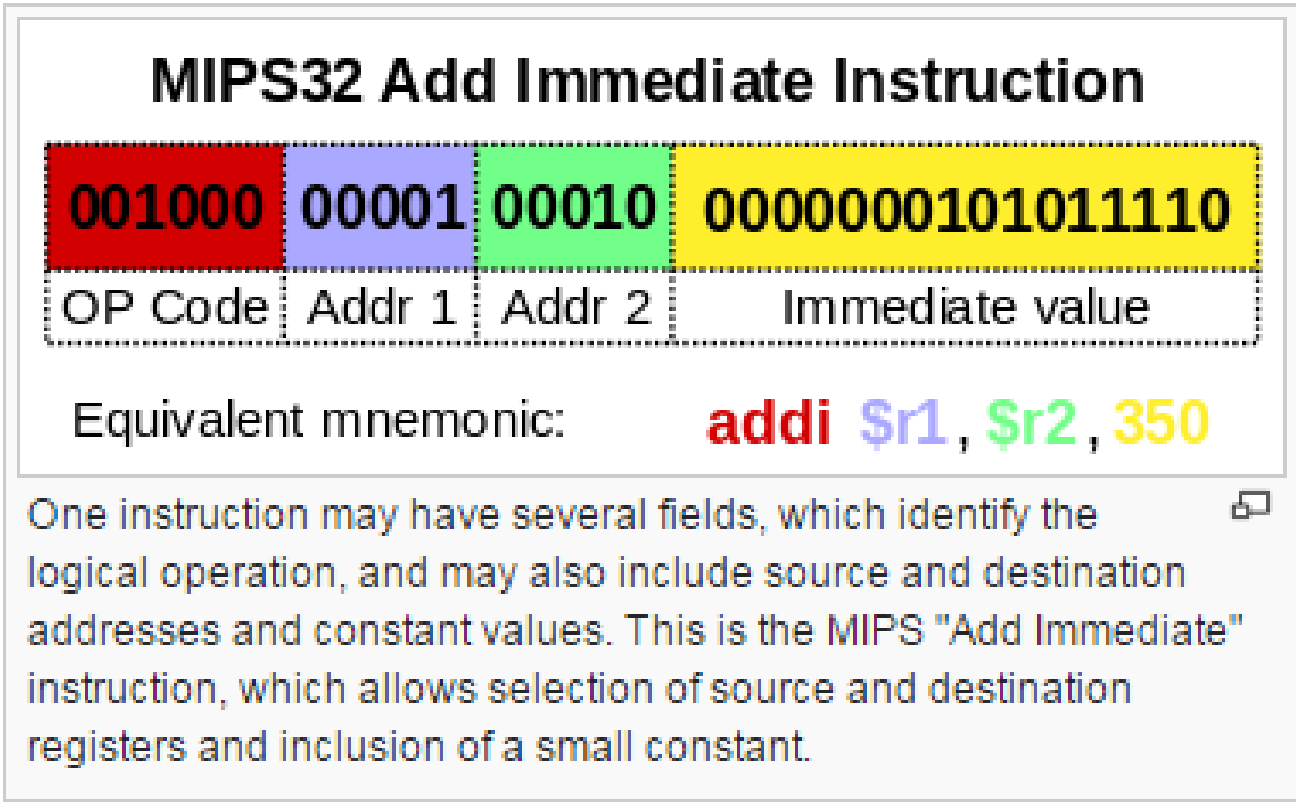
Instruction Set Architecture review

CMPE 311

Instruction Set

- An ISA includes a specification o
  the set of opcodes (machine
  language), and the native
  commands implemented by a
  particular processor



Source: wiki

RISC vs. CISC

- CISC (complex instruction set computer)
  - VAX, Intel X86, IBM 360/370, etc.
- RISC (reduced instruction set computer)
  - MIPS, DEC Alpha, SUN Sparc, IBM 801

CISC	RISC
Variable length instruction	Single word instruction
Variable format	Fixed-field decoding
Memory operands	Load/store architecture
Complex operations	Simple operations

Why RISC is used?

- Top 10 instructions for 8086

° Rank	instruction	Integer Average Percent total executed
1	load	22%
2	conditional branch	20%
3	compare	16%
4	store	12%
5	add	8%
6	and	6%
7	sub	5%
8	move register-register	4%
9	call	1%
10	return	1%
	Total	96%

RISC advantage over CISC

- Low complexity
  - Generally results in overall speedup
  - Less error-prone implementation by hardwired logic or simple microcodes
- VLSI implementation advantages
  - Less transistors
  - Extra space for the same area: more registers, cache
- RISC strategy also brings some very important advantages. Because each instruction requires only one clock cycle to execute, the entire program will execute in approximately the same amount of time
- Marketing
  - Reduced design time, less errors, and more options increase competitiveness

CISC Problems

- Performance tuning unsuccessful
  - Rarely used high-level instructions
  - Sometimes slower than equivalent sequence
- High complexity
  - Pipelining bottlenecks $\rightarrow$ lower clock rates
  - Interrupt handling can complicate even more
- Marketing
  - Prolonged design time and frequent microcode errors hurt competitiveness

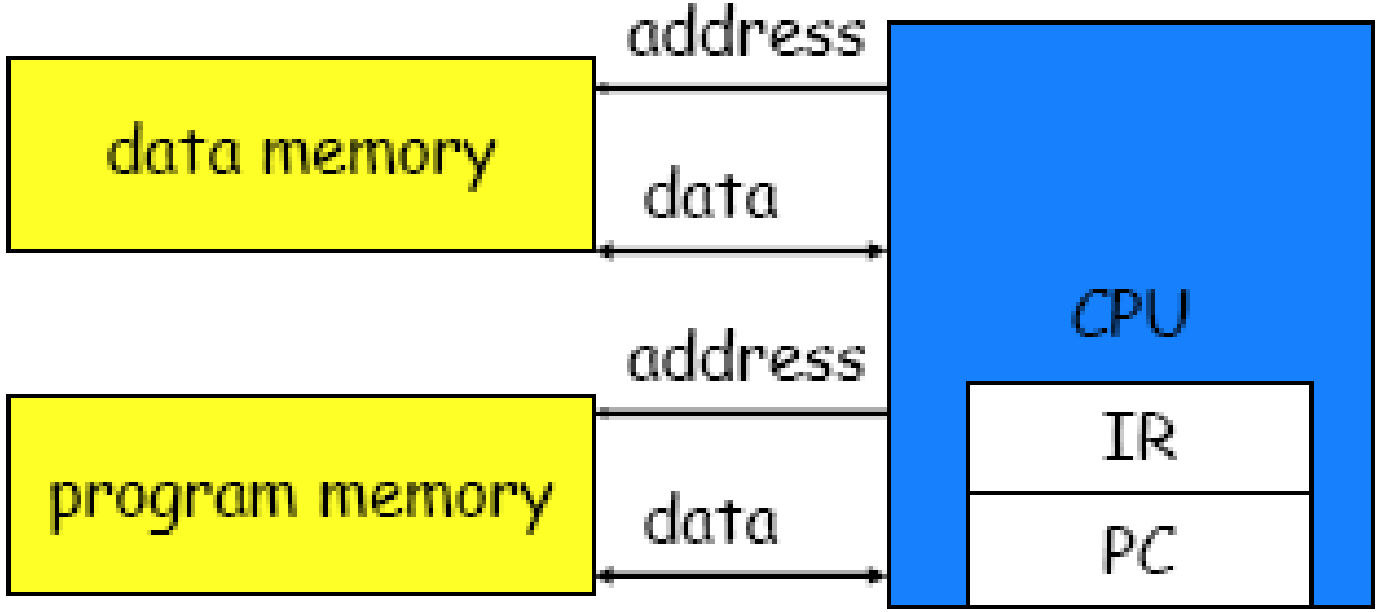
Harvard vs. Von Neumann Architecture

- The **Harvard architecture** is a computer architecture with physically separate storage and signal pathways for instructions and data.
- **Contrast with von Neumann architectures:**
  - Under pure von Neumann architecture the CPU can be either reading an instruction or reading/writing data from/to the memory. Both cannot occur at the same time since the instructions and data use the same bus system. In a computer using the Harvard architecture, the CPU can both read an instruction and perform a data memory access at the same time, even without a cache. A Harvard architecture computer can thus be faster for a given circuit complexity because instruction fetches and data access do not contend for a single memory pathway.

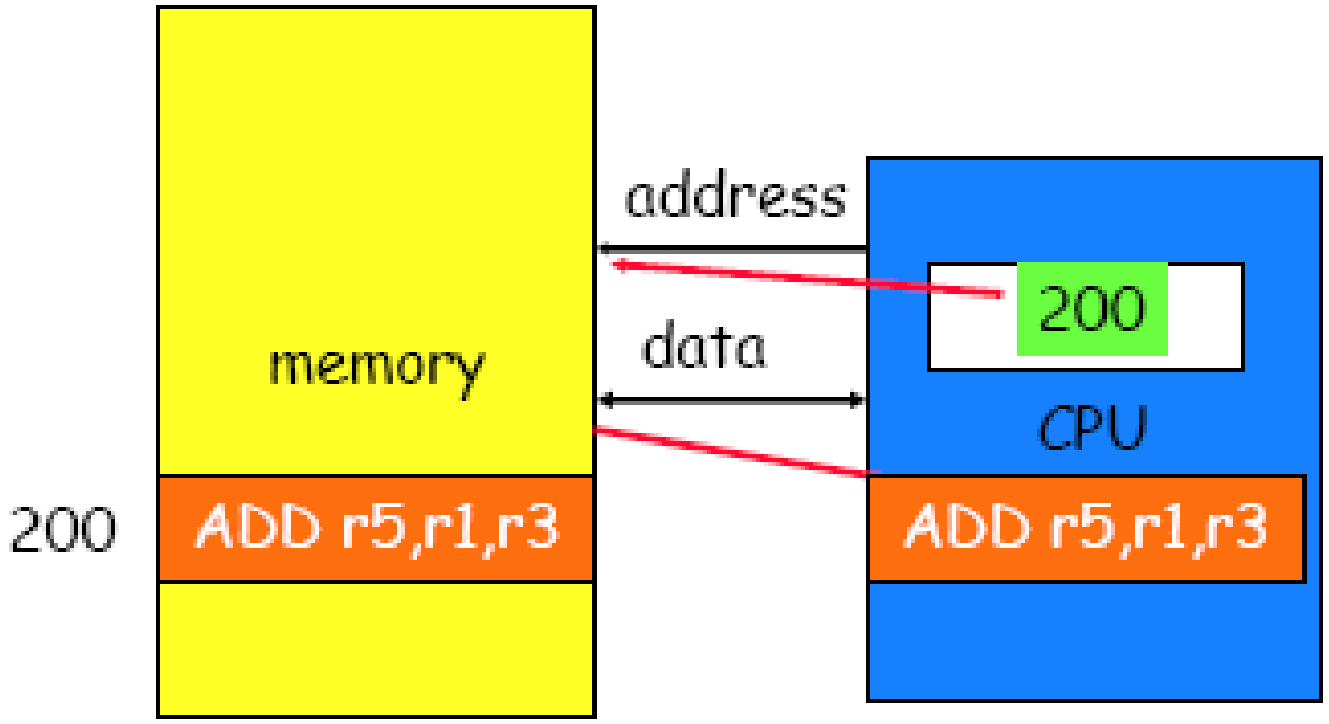
Von Neumann vs. Harvard

- von Neumann
  - Same memory holds data, instructions.
  - A single set of address/data buses between CPU and memory
- Harvard
  - Separate memories for data and instructions.
  - Two sets of address/data buses between CPU and memory

Harvard Architecture



Von Neumann



Acronyms and some definitions

- MIPS
- ISA
- Clk rate
- Clk cycle time or period